

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,800,947 B2
APPLICATION NO. : 09/893036
DATED : October 5, 2004
INVENTOR(S) : Sathe

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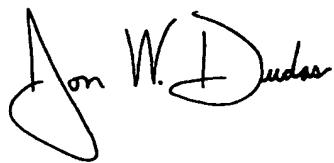
It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

The title page, showing an illustrative figure, should be deleted and substitute the attached title page.

Delete drawing sheet 3 and substitute the drawing sheet consisting of Fig 3 as shown on the attached page.

Signed and Sealed this

Twentieth Day of June, 2006



JON W. DUDAS
Director of the United States Patent and Trademark Office

(12) United States Patent
Sathe(10) Patent No.: US 6,800,947 B2
(45) Date of Patent: Oct. 5, 2004(54) FLEXIBLE TAPE ELECTRONICS
PACKAGING

(75) Inventor: Ajit V. Sathe, Chandler, AZ (US)

(73) Assignee: Intel Corporation, Santa Clara, CA
(US)(*) Notice: Subject to any disclaimer, the term of this
patent is extended or adjusted under 35
U.S.C. 154(b) by 0 days.

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Primary Examiner—Eddie Lee

Assistant Examiner—Quang Lu

(74) Attorney, Agent, or Firm—Schwegman, Lundberg,
Woessner & Kluth, P.A.

(57) ABSTRACT

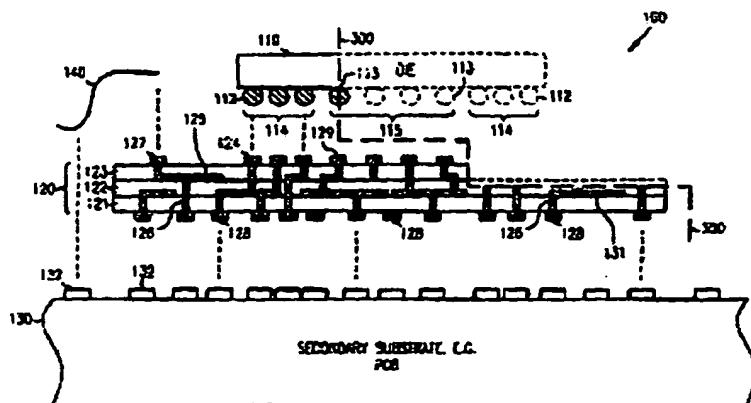
To decrease the weight and the thickness, and to increase the flexibility, of an electronics package, the package includes an integrated circuit (IC) mounted on a flexible tape substrate. In one embodiment, an IC is mounted on a flexible tape substrate using a ball grid array arrangement; however, other arrangements, including lead bonding, can be used. The flexible tape substrate can comprise conductive trances, vias, and patterns of lands on one or more layers. Methods of fabrication, as well as application of the flexible tape package to an electronic assembly, an electronic system, and a data processing system, are also described.

15 Claims, 12 Drawing Sheets

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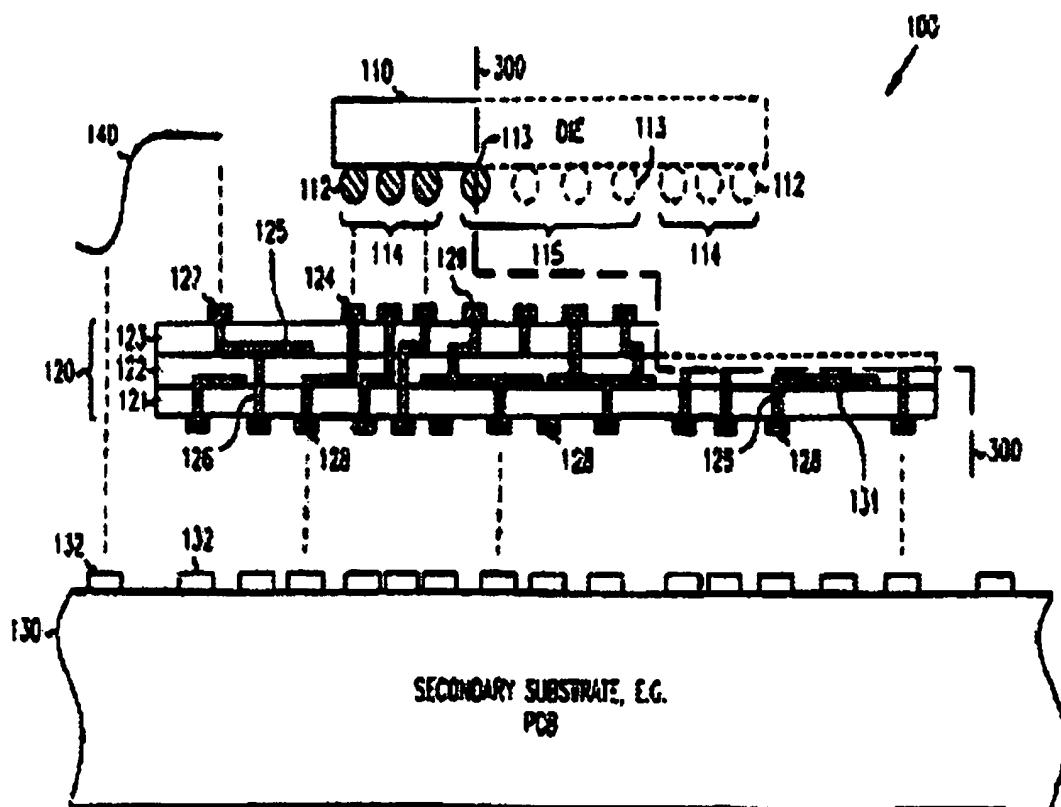


FIG. 3